CLAIMS

1. An apparatus, comprising:

a memory unit to store input data for a plurality of functions;

a control unit to control execution of said plurality of functions, said control unit to select a function to execute using a function identifier; and

a plurality of execution units operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier.

2. The apparatus of claim 1, wherein said execution units comprise a logic unit to perform scalar arithmetic operations, and at least one data path execution unit to perform arithmetic operations.

3. The apparatus of claim 1, further comprising a configuration memory to store configuration parameters for said control unit, said configuration parameters including a fuse map and table content data.

4. The apparatus of claim 3, wherein said control unit comprises:

a control unit state machine module to be configured in accordance with said fuse map, said control unit state machine to output an operation number address; and

a control unit lookup table to be configured with said table content data, said control unit lookup table to convert said operation number address to a reconfigurator

vector, said reconfigurator vector to control execution of said function by said execution units.

5. The apparatus of claim 4, wherein said control unit further comprises:

an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal;

an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal; and

a register file module to store a state for one function while another function is being executed by said execution units.

6. The apparatus of claim 5, wherein said control unit state machine module receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, and uses said inputs to generate said operation number address.

7. The apparatus of claim 1, further comprising a data selector to read said input data from said memory unit, and distribute said input data to said execution units.

8. The apparatus of claim 1, further comprising a register file module to store previously read input data during function execution when multiple read cycles are needed to provide data for said function.

9. The apparatus of claim 1, further comprising a data packer to receive processed input data from said execution units, and to send said processed input data to an output buffer.

10. The apparatus of claim 1, further comprising a data router adapter to communicate packets with said routing elements, said data router adapter to distribute data from received packets to a configuration memory or said memory unit, and transmit packets of processed data from said execution units stored in an output buffer.

11. The apparatus of claim 1, wherein said logic unit comprises a data address generator to control writing said input data to said memory unit, and reading said input data from said memory unit.

12. A system, comprising:

an antenna;

a host processing system;

a configuration module; and

a reconfigurable communication architecture module operatively responsive to said configuration module, said reconfigurable communication architecture module to receive said configuration information and configure itself to execute a plurality of applications in accordance with said configuration information.

13. The system of claim 12, wherein said reconfiguration communication architecture module comprises:

a plurality of processing elements, with each processing element to execute at least one function for said application;

a plurality of routing elements to connect said processing elements; and

a plurality of communications media to connect said processing elements and said routing elements in a mesh topology.

14. The system of claim 13, wherein one of said processing elements comprises:

a memory unit to store input data for a plurality of functions;

a control unit to control execution of said plurality of functions, said control unit to select a function to execute using a function identifier;

a plurality of execution units operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier.

15. The system of claim 14, wherein said execution units comprise a logic unit to perform scalar arithmetic operations, and at least one data path execution unit to perform arithmetic operations.

16. The system of claim 14, further comprising a configuration memory to store configuration parameters from said configuration information for said control unit, said control unit to generate control signals in accordance with said configuration parameters.

17. A method, comprising:

receiving configuration information;

configuring a control unit using said configuration information;

receiving input data for a plurality of functions;

controlling execution of said plurality of functions using control signals; and

executing said plurality of functions by a plurality of execution units using said input data in accordance with said control signals.

18. The method of claim 17, wherein said plurality of functions are executed during different time periods.

19. The method of claim 17, wherein said configuring comprises:

receiving configuration parameters for said control unit, said configuration parameters to include a fuse map and table content data;

configuring a control unit state machine module using said fuse map; and

configuring a control unit lookup table using said table content data.

20. The method of claim 17, wherein said controlling comprises:

reading a function identifier for a function from a function list;

generating a reconfigurator vector using said function identifier;

sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector; and

sending function control signals to said execution units to process said input data in accordance with said reconfigurator vector.

21. The method of claim 20, wherein said generating comprises:

receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine;

generating an operation number address using said inputs; and

converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units.

22. The method of claim 17, wherein said executing comprises:

receiving said input data at said execution units;

receiving function control signals from said control unit; and

processing said received input data in accordance with said function control signals.

23. The method of claim 17, wherein said receiving comprises:

receiving a function identifier and an input identifier for each function;

creating an input buffer corresponding to each input identifier; and

writing input data for each function in said corresponding input buffer.

24. An article comprising:

a storage medium;

said storage medium including stored instructions that, when executed by a processor, result in receiving configuration information, configuring a control unit using said configuration information, receiving input data for a plurality of functions, controlling execution of said plurality of functions using control signals, and executing said plurality of functions by a plurality of execution units using said input data in accordance with said control signals.

25. The article of claim 24, wherein the stored instructions, when executed by a processor, further result in said plurality of functions being executed during different time periods.

26. The article of claim 24, wherein the stored instructions, when executed by a processor, further result in said configuring by receiving configuration parameters for said control unit, said configuration parameters to include a fuse map and table content data, configuring a control unit state machine module using said fuse map, and configuring a control unit lookup table using said table content data.

27. The article of claim 24, wherein the stored instructions, when executed by a processor, further result in said controlling by reading a function identifier for a function from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in

accordance with said reconfigurator vector, and sending function control signals to said execution units to process said input data in accordance with said reconfigurator vector.

28. The article of claim 27, wherein the stored instructions, when executed by a processor, further result in said generating by receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine, generating an operation number address using said inputs, converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units.

29. The article of claim 24, wherein the stored instructions, when executed by a processor, further result in said executing by receiving said input data at said execution units, receiving function control signals from said control unit, and processing said received input data in accordance with said function control signals.

30. The article of claim 24, wherein the stored instructions, when executed by a processor, further result in said receiving by receiving a function identifier and an input identifier for each function, creating an input buffer corresponding to each input identifier, and writing input data for each function in said corresponding input buffer.